REMARKS

Claim Rejections

Claims 1-7 are rejected under 35 U.S.C. § 112, second paragraph. Claims 1-7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kato et al. (U.S. 5,589,406) in view of Hasegawa (U.S. 2004/0026738).

Substitute Specification

As required by the Examiner, a Substitute Specification is enclosed, along with a marked-up copy of the original specification indicating the changes made thereto by the Substitute Specification. No "new matter" has been added to the original disclosure by the Substitute Specification. Entry of the Substitute Specification is respectfully requested.

Abstract of the Disclosure

Applicant is submitting a substitute Abstract of the Disclosure for that originally filed with this application to more clearly describe the claimed invention. Entry of the Substitute Abstract of the Disclosure is respectfully requested.

Drawings

Applicant has amended Figures 1-7, as illustrated on the attached formal drawings, accompanied by a LETTER TO THE OFFICIAL DRAFTSPERSON. Figure 1 was amended to correct the reference line for reference number "6",and the words "Wet Etching" were deleted.. Figure 2 was amended to properly identify reference line with reference numbers "1", "2", "3", "3a", "4", "7", and "8", and the words "Dry Etching" were deleted. Figure 3 was amended to add reference number "15", and the words "Excimer Laser Recrystallization" and "Direction of Grain Growth" were deleted. Figure 4 was amended to replace the words with reference numbers --7--, --10--, --11--, and --12--. Figure 5 was amended to replace the words with reference number --7--. Figure 6 was amended to replace the words with reference numbers --7--, --13--, and --14--. Figure 7 was amended to replace the words with reference numbers --7--, --10--, --11--, and --12--, and add the label --

SUBSTITUTE SPEC
10/601,701

Method for Fabrication of Polycrystalline Silicon Thin Film Transistors

~~Reference cited~~

~~1. U.S.A. Patent No:6,495,405.~~

~~2. U.S.A. Patent No:5,395,481.~~

~~3. U.S.A. Patent No:5,021,119.~~

~~4. U.S.A. Patent No:4,330,363.~~

~~5. U.S.A. Patent No:4,592,799.~~

~~6. Ching-Wei Lin et. al. "High-performance low-temperature Poly-si TFTs crystallized by excimer laser irradiation with Recessed-Channel-Structure", IEEE Electron Devices Lett., vol.22, pp.269-271, 2001.~~

~~7. G. K. Giust et al., "Performance improvement obtained for thin-film transistors fabricated in prepatterned laser recrystallized polysilicon", IEEE Electron Devices Lett., vol.18, pp.296-298, 1997.~~

~~8. G. K. Giust et. al., "Comparison of excimer laser recrystallized prepatterned and unpatterned silicon films on SiO_2", J. Appl. Phys. 81, pp.1204-1214,1997.~~

~~9. Yasuyuki Sano et. al., "High-performance single-crystalline-silicon TFTs on a non-alkali-glass substrate", in Tech. Dig. IEDM, 2002.~~

Field of the invention

The present invention relates to a method for manufacturing polycrystalline silicon thin film transistors with a ~~for method of~~ laser-recrystallized active layer. More particularly, the present invention ~~form~~ forms a large silicon grain structure of the active layer without an ~~any~~

additional mask.

Description of the Prior Art

~~Background of the Invention~~

In growing the thin film transistor display from a low temperature polycrystalline silicon thin film transistor (LTPS-TFT) extending over an amorphous silicon thin film transistor (a-si TFT), it has been proposed to use various conventional display devices, such as, personal digital assistant, digital camera, cell phone so as to substantially enhance resolution, brightness, size and electromagnetic disturbance by LTPS-TFT display.

However, such conventional laser annealing LTPS-TFTs process has proven to be unsatisfactory. When forming the active layer of transistor after the laser recrystallization is ~~are~~ used to fabricate LTPS-TFTs, the resulting silicon grain structure typically lacks uniform structure. Such nonuniformity is due to the small and irregular silicon grain which causes the difference of electric characteristic between elements. But, when the laser recrystallization are formed after ~~after forming~~ the active layer of transistor are used to fabricate LTPS-TFTs, the resulting surface tension causes ~~induced~~ shrinkages, which are caused by melting the silicon film. Therefore, the conventional method can not be used to produce ~~use to process of~~ LTPS-TFTs.

The structure of a TFT and silicon-on-insulator metal oxide semiconductor field effect transistor (SOI-MOSFET) is an insulated layer with poor thermo conductivity under the active layer. When a working current of the device is large ~~to suddenly cause~~ high temperature in the ~~of~~ active layer can suddenly be produced, such that a carrier of the active layer is ~~to diminish~~ diminished, that the relative study reports the division of channel W into parallel connection of many small channels W to overcome

self-heating effect as shown in FIG.7. It shows a conventional view of settlement of self-heating effect. More particularly, ~~such~~ the conventional division of channel W into the parallel connection of many small channels W_i cannot be sufficiently overcome by dispersing heat during the large working current ~~so that the new invention is desirable~~, unlike the present invention.

Summary of the invention

Accordingly, the present invention discloses a method for fabrication of polycrystalline silicon thin film transistors, which comprises a polysilicon spacer capping onto ~~the~~ a sidewall of the active layer in thin film transistors by an isotropic dry etching process for silicon film.

Therefore, the present invention provides uniform arrangement of grain boundaries and large grain sizes of active layer.

The main object of the present invention is to provide high mobility of a field effect carrier of a low temperature polycrystalline silicon thin film transistor (LTPS-TFT) and diminish a difference between the devices. Therefore, the resolution of display is substantially improved ~~promote~~ by the present invention on a pixel of the driving transistor to form small channel width have large silicon grain structure. Moreover, the laser-recrystallized process window is substantially broad to improve the ~~promote device~~ performance and uniformity of the device.

The other object of this invention is ~~to trigger the no~~ the benefit of not requiring an additional mask ~~of~~ for recrystallization of the ~~melting~~ melted lateral silicon after excimer laser annealing and ~~improve~~ improving the self-heating effect caused by dispersing the heat of the high working current. The fabrication of polycrystalline silicon thin film transistors employ high energy continuous wavelength laser on a dog-bone shape shaped active

layer by source-drain directional scanning to improve the channel of the transistor of a silicon grain and then to have high performance and good uniformity.

A method for fabrication of polycrystalline silicon thin film transistors comprising the steps of:

a) selecting a substrate;

b) forming a buffer oxide ~~formed~~ on the substrate;

c) depositing a amorphous silicon film on the buffer oxide;

d)depositing a low-temperature oxide on the amorphous silicon film, wherein the low temperature oxide ~~is employed to form~~ forming a stop layer of silicon film dry etching after step d) process, a thermal insulating layer of laser annealing or a hard mask of the removal of polysilicon spacer after recrystallization;

e) ~~forming~~ etching the amorphous silicon film by photoresist ~~of~~ utilizing a hard mask on the low temperature polycrystalline silicon thin film transistor (LTPS-TFT) as a active layer, and then using a solution of silicon dioxide of wet isotropic etching to slightly ~~go toward~~ perform an inner etching of the buffer oxide before or after the removal of the hard mask;

f) depositing another amorphous silicon film by connecting the active layer, and then forming the polysilicon spacer by dry etching behind either side of the active layer of the low temperature polycrystalline silicon thin film transistor (LTPS-TFT) , and then forming large silicon grain structures of the active layer by recrystallization of high-energy continuous wavelength laser or recrystallization of excimer laser annealing on dog-bone shape active layer.

Brief description of the drawings

The present invention will be better understood from the following detailed description of preferred embodiments of the invention, taken in conjunction with the accompanying drawings, in which :

FIG. 1 ~ FIG. 3 are schematic cross sections of the essential portion illustrating a process for manufacturing polycrystalline silicon thin film transistors according to the present invention;

FIG. 4 is a schematic top plan view of relative position showing the laser-recrystallized active layer for polycrystalline silicon thin film transistors according to the present invention;

FIG. 5 is a scanning electron microscope (SEM) of silicon grain structures after excimer laser annealing (ELA) with silicon film thickness at 500 angstrom and line width at 2 microns according to the present invention;

FIG. 6 is a schematic view showing active layer position and scanning direction of continuous-wavelength laser for recrystallization continuous-wavelength laser according to the present invention; and

FIG. 7 is a conventional view of settlement of self-heating effect.

Description of the preferred embodiments

The following descriptions of the preferred embodiments are provided to understand the features and the structures of the present invention.

~~Please referring to the FIG. 1 ~ FIG. 3, that~~ Figs. 1-3 are schematic cross sections of ~~the~~ an essential portion illustrating a process for polycrystalline silicon thin film transistors comprising the steps of:

a) selecting a substrate 1;

b) forming a buffer oxide 2 ~~formed~~ on said substrate 1;

c) depositing a amorphous silicon film 3 on the buffer oxide2;

d) depositing a low temperature oxide 4 on the amorphous silicon film 3, wherein the low temperature oxide 4 forming ~~is employed to form~~ a stop layer of silicon film dry etching after step d) process, a thermal insulating layer of laser annealing or a hard mask of the removal of polysilicon spacer after recrystallization;

e) etching the ~~forming~~ amorphous silicon film 3 by photoresist 5 utilizing a of hard mask on the low temperature polycrystalline silicon thin film transistor (LTPS-TFT) as a active layer, and then using a solution of silicon dioxide 6 of wet isotropic etching to slightly go toward inner etching of the buffer oxide 2 before or after the removal of the hard mask;

f) depositing another amorphous silicon film 3a by connecting the amorphous silicon film 3, and then forming the polysilicon spacer 7 by dry etching 8 on either side of the another amorphous silicon film 3a and the amorphous silicon film 3. The polysilicon spacer 7 is selected from the group consisting of polycrystalline silicon film and amorphous silicon film. The polysilicon spacer 7 can replace the dielectric material with oxide, nitride, and metal oxide, etc. and metal material with aluminum (Al), wolfram (W), molybdenum (Mo) and chromium (Cr), etc.. And then can ~~choice~~ choose to cancel the polysilicon spacer 7 or not for the next process. The polysilicon spacer 7 ~~form~~ formed behind either side of the active layer (amorphous silicon film 3) of the low temperature polycrystalline silicon thin film transistor (LTPS-TFT) , and then form large silicon grain structures of the active layer according to a direction of grain growth is by recrystallization of high-energy continuous wavelength laser or recrystallization of excimer laser annealing 9 on dog-bone shape active layer as shown in FIG. 3.

Therefore, the active layer generates a temperature gradient.

The polysilicon spacer 7 is formed on either side of the active layer ~~of selecting from the~~ selected from a group consisting of a thin film transistor (TFT) and a silicon-on-insulator metal oxide semiconductor field effect transistor (SOI-MOSFET) in a low temperature or high temperature process. The polysilicon spacer 7 ~~further comprises~~ is located under either side of the active layer.

The main object of the polysilicon spacer 7 on laser-recrystallized either side of the active layer of the thin film transistor (TFT) is to generate a temperature gradient for recrystallization of the active layer. Moreover, the order of the steps for forming the polysilicon spacer 7 and recrystallization of the active layer can change, forms recrystallization of active layer by selecting from the group consisting of excimer laser annealing (ELA), solid phase crystallization (SPC) or metal-induced lateral crystallization (MILC) , and then forming the polysilicon spacer 7 on either side of said active layer of the thin film transistor (TFT) or silicon-on-insulator metal oxide semiconductor field effect transistor (SOI-MOSFET).

Fig 4

~~Please seeing the FIG.4,~~ It shows the relative position of gate 10, source 11, and drain12 to be surrounded the side of active layer (amorphous silicon film 3) by the polysilicon spacer 7. Next, FIG. 5 is a scanning electron microscope (SEM) of silicon grain structures with silicon film thickness at 500 angstrom and line width at 2 microns after excimer laser annealing (ELA). It is clear that the elongated silicon grains measure over 1 micron with direction to side of active layer. Because the laser can't melt the thick boundary of active layer and can easily melt thin channel, and then the silicon grain trigger inner recrystallization by the spacer seed of the polysilicon spacer 7. Moreover, it also efficiently overcomes shrinkage effect

of active layer caused by surface tension after melting of silicon film. Thus, the present invention is to efficiently improve the self-heating effect by forming a thick polysilicon spacer 7 ~~of no~~ with out an extra mask on a side of the ~~small wide~~ channel. FIG. 6 is a schematic view showing the active layer position and scanning direction of continuous-wavelength laser for recrystallization of with a dog bone shape 13 a 14 a utilizing the continuous-wavelength laser according to embodiment of the present invention.

The present invention may be embodied in other specific forms without departing from the spirit of the essential attributes thereof, therefore, the illustrated embodiment should be considered in all respects as illustrative and not restrictive, reference being made to the appended claims rather than to the foregoing description to indicate the scope of the invention.